

Media Codec FTMCP100

Key Features

- Support AHB 2.0 interface
- Compliant with MPEG-4 (ISO/IEC 14496-2) simple profile L0 ~ L3 standard, with resolutions including subQCIF, QCIF, CIF, VGA and 4CIF @ 30 fps, with a step of 16
- Compliant with JPEG (ISO/IEC 10918-1) base-line standard
- Include a capture interface supporting ITU 656 YUV 4:2:2 input format
- Include hardware engines for Motion Estimation/ Motion Compensation, DCT / IDCT, Quantization / Inverse Quantization, AC / DC prediction and Variable Length Coding / Decoding
- A local memory controller to control local memory shared by CPU, FTMCP100 and DMA master
- A DMA controller to control data transfers between system memory and local memory
- Automatic power down mechanism to reduce power consumption
- Motion Estimation search range: -16 ~ +15.5 (optionally -32 ~ +31) with half-pel accuracy
- Support 4MV and unrestricted MV
- Rate control: constant bit rate control and variable bit rate control
- Error resilient tools: encoder supports resynchronization marker and header extension code; decoder supports resynchronization marker, header extension code, data partition and RVLC
- Support short video header (H.263 baseline)
- Support H.263/MPEG/JPEG quantization methods
- JPEG supported features:
 - support 4 user-defined Huffman tables (2AC and 2DC)
 - support 4 programmable quantization tables
 - support interleave and non-interleave scans
 - support YUV 4:4:4, 4:2:2 and 4:2:0 formats
 - support image size up to 64k × 64k
- Support full-duplex operation (e.g. video phone and video conference) by s/w switching encoding and decoding task on the same h/w

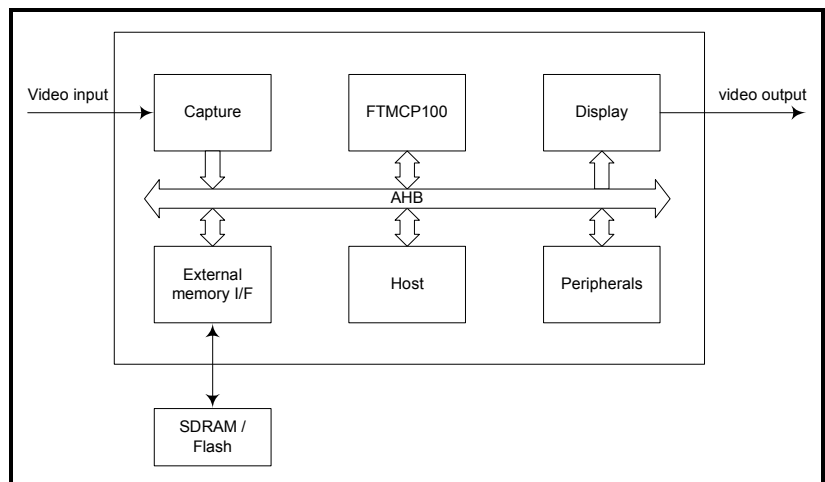
General Description

The FTMCP100 is a video and image compression/decompression IP core supporting MPEG-4 (ISO/IEC 14496-2) and JPEG (ISO/IEC 10918-1) related applications. The FTMCP100 includes some hardware engines to accelerate computation intensive tasks such as Motion Estimation / Motion Compensation, DCT / IDCT, Quantization / Inverse Quantization, AC / DC prediction, Zigzag Scan and Variable Length Coding / Decoding. The FTMCP100 can be controlled by a CPU through AHB 2.0 interface. By initializing the control registers of the FTMCP100, the Motion Estimation and encoding/decoding pipeline for a macroblock can be done automatically. Thus CPU can be released from timing critical tasks in video and image encoding/decoding. The single-phase clock and standard-cell based approach allows you to quickly integrate the FTMCP100 into your SoC designs.

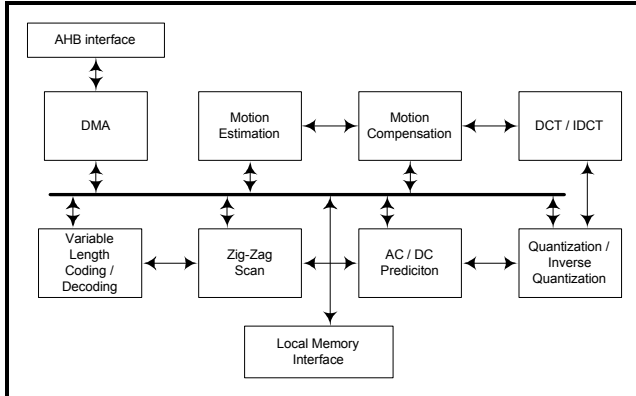
Applications

- Surveillance & monitoring systems
- Video phone and video conference
- Digital cameras and digital camcorders
- IP cameras
- Mobile phones
- PDAs
- PVRs, STBs
- MPEG-4 recorders/players

System Diagram



Functional Blocks



Block Descriptions

Video Capture Interface

The video capture interface performs the task of transferring video data from ITU 656 input format to the system memory. The video capture interface comprises an AMBA AHB compatible master interface for transferring video data to the system memory, an AMBA AHB compatible slave interface for accessing the control registers of the video capture interface. The capture interface supports various video resolutions including QCIF, CIF and D1.

AHB Interface

The AHB interface consists of AHB master and slave interface. The AHB master interface is used by DMA to control data transfer between system memory and local memory. The AHB slave interface is used by CPU to control FTMCP100 operation.

DMA

The DMA controller performs the task of transferring data between the system memory and the local memory of FTMCP100. The main function of the DMA controller is data movement and translation to a format suitable for processing by other hardware engines.

Motion Estimation

The Motion Estimation (ME) unit can do motion estimation for the entire search window based on a fast search algorithm. By reading commands in local memory, the motion estimation for a macroblock can be completed automatically.

DCT / IDCT

The DCT / IDCT unit is responsible for Discrete Cosine Transform and Inverse Discrete Cosine Transform. The IDCT unit uses the same hardware resources as the DCT unit. The IDCT results are compliant with IEEE 1180-1990 spec. During encoding phase, the DCT results are passed to Quantization unit, whereas during decoding phase, the IDCT results are passed to MC unit.

Quantization / Inverse Quantization

The Quantization / Inverse Quantization unit supports H.263/MPEG / JPEG quantization methods. During encoding phase, the quantization results are passed to AC/DC prediction unit, whereas during decoding phase, the inverse quantization results are passed to IDCT.

AC/DC Prediction

The AC/DC prediction unit supports MPEG-4 AC/DC prediction method and JPEG DC prediction method. During encoding phase, the AC/DC prediction results are passed to Zigzag Scan unit, whereas during decoding phase, the inverse AC/DC prediction results are passed to Inverse Quantization unit.

Zigzag Scan

The Zigzag Scan unit supports all MPEG-4 scan methods and JPEG zigzag method. During encoding phase, the zigzag results of (run, level) pairs are passed to VLC unit, whereas during decoding phase, the inverse zigzag results are passed to AC/DC Prediction unit.

Variable Length Coding/Decoding

The Variable Length Coding/Decoding (VLC/VLD) unit supports MPEG-4 fixed variable length codes and JPEG user-defined Huffman codes. During encoding phase, the VLC results are final compressed bitstreams, whereas during decoding phase, the VLD results are passed to Zigzag unit.

Motion Compensation

The Motion Compensation (MC) unit is an engine responsible for motion compensation task. During encoding phase, it subtracts the interpolated block from the current block and sends the residual block to DCT. During decoding phase, it adds the interpolated block to the IDCT output block to get the reconstructed block.

Local Memory Controller

The local memory controller arbitrates local memory access requests from CPU, DMA, and FTMCP100. The local memory controller supports several addressing modes to achieve optimum utilization of the local memory bandwidth.

Signal Descriptions

The FTMCP100's signals can be divided into the following groups:

- AHB interface signals
- Memory interface signals

CODEC Signals

| Signal Name | In / Out | Description |
|-------------|----------|---------------------------|
| CPCLK | In | Codec clock input |
| GRST | In | Global reset, active HIGH |
| mcp_int | Out | Codec interrupt output |

AHB Interface Signals

| Signal Name | In / Out | Description |
|-------------|----------|------------------------------|
| HCLK | In | Bus clock |
| HRESETn | In | Bus reset |
| HBUSREQ | Out | Bus request |
| HLOCK | Out | Bus lock |
| HGRANT | In | Bus grant |
| mHADDR | Out | Master address bus |
| mHTRANS | Out | Master transfer type |
| mHWRITE | Out | Master transfer direction |
| mHSIZE | Out | Master transfer size |
| mHBURST | Out | Master burst type |
| mHPROT | Out | Master protection control |
| mHWDATA | Out | Master write data bus |
| mHRDATA | In | Master read data bus |
| mHREADY | In | Master transfer done |
| mHRESP | In | Master transfer response |
| mCMDOE | Out | Master command output enable |
| mDATOE | Out | Master data output enable |
| sHADDR | In | Slave address bus |
| sHTRANS | In | Slave transfer type |
| sHWRITE | In | Slave transfer direction |
| sHSIZE | In | Slave transfer size |
| sHBURST | In | Slave burst type |
| sHWDATA | In | Slave write data bus |
| sHRDATA | Out | Slave read data bus |
| HSEL | In | Slave select |
| sHREADY | Out | Slave transfer done |
| sHREADYin | In | System transfer done |
| sHRESP | Out | Slave transfer response |
| sRESPOE | Out | Slave response output enable |
| sDATOE | Out | Slave data output enable |

For a complete definition and / or description of any or all signal(s), please refer to the FTMCP100 Data Sheet.

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