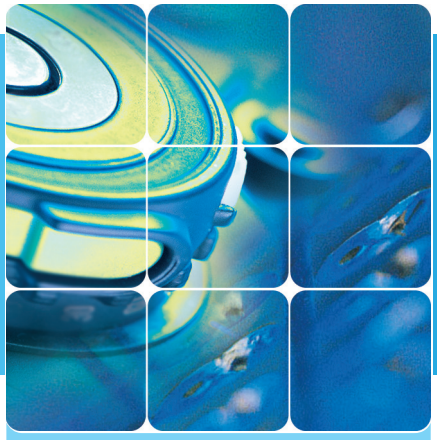
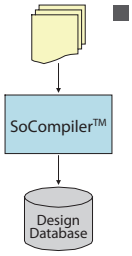


SoCompiler™ Design Services

A Powerful Platform-based Design Service for SoCs

Highlights

- Dedicated SoCompiler™ consultant to help:
  - SoC specification
  - IP configuration
  - Application/software development
- Automated, platform-based SoCompiler™ toolset that:
  - Integrates IPs for AMBA 2.0 & 3.0 spec
  - Generate test bench and constraint files
  - Verify the SoC design
  - Prepare the SoC design for implementation
  - Generate RTL integration and test bench for FPGA verification



SoCompiler™ Data Flow

- SoC design intent, including:
  - System resource mapping
  - IP connectivity
  - Pin mapping
- Complete integrated SoC design database:
  - RTL top-level integration
  - Verification environment
  - Synthesis environment
  - FPGA environment

FARADAY

Reduce Time-to-Market for ARM-based SoCs

The increasing complexity of SoCs has resulted in longer design cycles. SoC designers are spending most of their resources on specification, integration and verification due to IP and chip-level issues. Faraday SoCompiler™ Design Services can help reduce the frontend SoC design time by leveraging an innovative in-house tool that quickly realizes customers' design intent and provides a comprehensive verification environment to help reduce risk.

Faraday's SoCompiler™ Design Services

Faraday's SoCompiler™ Design Services leverage our 20 years of experience in the IP and ASIC design service businesses. Faraday's SoCompiler™ Design services provide customers a winning combination with the largest IP selection in UMC processes, SoC design experience, an integrated design flow that makes the most out of automation and a correct by design methodology.

SoCompiler™ Consultants

Faraday SoCompiler™ consultants are experienced engineers familiar with all levels of design, from SoC architecture, to IP and physical implementation. Involved at the initial specification stage all the way to tape-out, SoCompiler™ consultants can be counted on to provide guidance on SoC architectural trade-offs, selecting and configuring the right IPs, and offering suggestions during synthesis to help reduce implementation time.

SoCompiler™ Tool Automation

Faraday's automated, platform-based design tool quickly integrates IPs circuits to provide customers with a top-level design and the FPGA verification environment.

SoCompiler™ Specification

Faraday SoCompiler™ consultants will work with customers to finalize their design specification, generating a functional block diagram to visually construct the design, and preparing the design database for integration. An example SoC functional block diagram is shown in Figure 1 below.

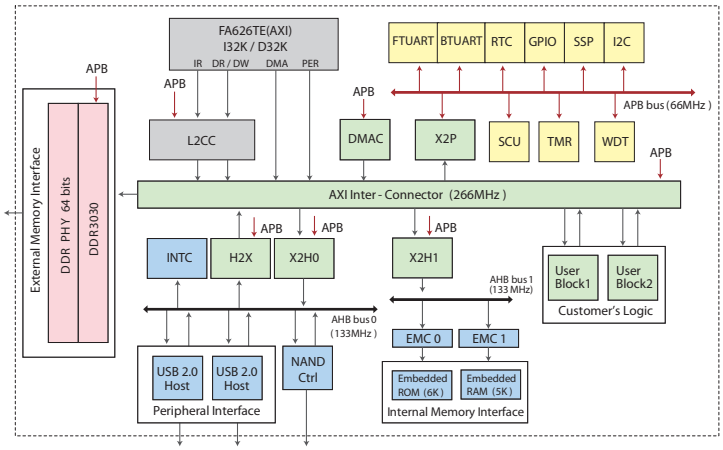


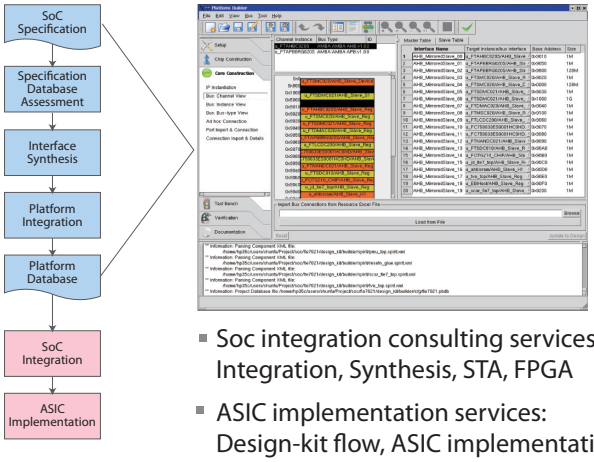
Figure 1. ARM-based SoC functional block diagram

SoCompiler™ Design Services
A Powerful Platform-based Design Service for SoCs

SoCompiler™ Integration
Once the design database is completed, SoCompiler™ consultants will begin running the automated integration tool, taking 2 weeks for typical designs.

SoCompiler™ Verification
The design database also allows SoCompiler™ consultants to generate the verification environment quickly and reliably, ensuring that all IPs circuits have been properly connected, taking 2 weeks for typical designs.

SoCompiler™ FPGA Generation
After the design integration and verification, SoCompiler™ allows SoC consultant to generate FPGA integration and verification environment for customer, taking 1 week for typical designs.

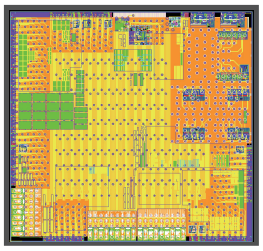


- Soc integration consulting services: Integration, Synthesis, STA, FPGA
- ASIC implementation services: Design-kit flow, ASIC implementation

Figure 2. SoCompiler™ design flow

SoCompiler™ Design Results
Released in early 2006 and continually updated, SoCompiler™ dramatically reduces SoC front-end design time to as short as 4 weeks even for today's largest designs. Following Faraday's SoCompiler™ design flow, customers can be assured of consistent, quality handoffs and deliverables at every stage of the design. Figure 3 shows an example of a successful SoC design using Faraday SoCompiler™ design services. The 300 million gate design took about 1 year from design start to tape-out, requiring about 4 weeks delivering the 1st integrated design database, including top-level RTL codes and verification suites.

Figure 3. A successful SoC design using Faraday's SoCompiler™ service



- SoC project details:
  - Logic gate count: over 100 million
  - Total gate count: over 300 million
  - System bus frequency : 400MHz
  - DDR3 data rate : 1.3GHz

Note: For customer confidentiality, a Faraday testchip of similar complexity is shown above for illustration purpose.

Driven by a company-wide commitment to servicing customers and fostering relationships, SoCompiler™ design services represent the next evolution in Faraday's pursuit of uncompromising ASIC design service; promising lower design risks and faster time-to-profit. With the unbroken track record of 100+ successful customer SoC tape-outs, Faraday is your trusted SoC partner!

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